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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/536,719	05/27/2005	Hirotaka Ochi	28951.5391	2212

27890 7590 10/28/2008

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EXAMINER	
STEVENS, BRIAN J	

ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
10/28/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/536,719	OCHI, HIROTAKA	
	Examiner	Art Unit	
	Brian J. Stevens	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,11,12 and 14* is/are rejected.

7)☒ Claim(s) *4,5,7-10 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 May 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is in response to Application No. 10/536,719 filed on May 27th, 2005. The amendments presented on August 12th, 2008 which provides changes to claims 1, 2, 4, 6-9 and 11-14 is hereby acknowledged. Claims 1-14 remain pending.

Allowable Subject Matter

2. Claims 4, 5, 7, 8, 9, 10 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

3. The objection to the claims for an allegedly improper claim order, has taken official notice, and hereby withdrawn.

4. Amendment to claim 14 in response to the rejection under 35 U.S.C. 112 has been considered. The amendment to the claim obviates previously raised rejection; as such this rejection is hereby withdrawn.

5. Applicant's arguments with respect to claims 1, 3 and 11 have been considered but are moot in view of the new ground(s) of rejection.

6. Applicant's arguments with respect to claims 2, 6 and 12 have been considered but are moot in view of the new ground(s) of rejection.

7. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

8. Applicant's arguments, see page 12 and 13 of remarks, filed August 8th, 2008, with respect to claim 8 have been fully considered and are persuasive. The rejection of claim 8 has been withdrawn.

9. Regarding claim 14, as rejected under 35 U.S.C. 103 as being obvious over applicant admitted prior art in view of Rakib et al, it is argued (Pages 13 and 14 of remarks) that the applied references do not teach claim limitations of claim 14, specifically a *phase synchronization device*, a *memory for storing tap factors*, and a *status change factor supply device*.

10. In response to the above-mentioned argument, applicant's interpretation of the prior art has been considered but they are not persuasive. The applicant admitted prior

art discloses having a frequency threshold device (See Figure 4, [402]) as agreed upon by the applicant. The frequency threshold device for judging frequency information of said phase synchronization device in a plurality of statuses using one or more threshold values (See Paragraph [0073]). Although the applicant is correct when stating "information on the size and direction of the phase error can be obtained" is expressed in the paragraph, through the use of status changes and phase error, frequency information can be found. For example, how many phases pass through a certain point in time would determine the frequency, thus by having the information of the amplitude or phases can in fact be used to obtain frequency information.

11. In response to the above-mentioned argument, applicant's interpretation of the prior art has been considered but they are not persuasive. The applicant admitted prior art discloses a status change factor supply device (See Figure 8, [802]) for supplying the tap factors (See Paragraph [0007]) corresponding to said "status" (Output) to said first digital equalization device (See Figure 8, [102] where the output is sent to [802] via [1031]). Although as stated by the applicant that the AAPA contains no disclose that the temporary factor computation means supply reacts to a change in a frequency information threshold device, the signal is still being sent to [802] for a specific reason. Since the output of [1031] is being sent to [802] and although no discloser is present, one would assume that the signal is being sent to the next stage because in fact it was being used. Since the output [1031] is for comparing to frequency information thresholds, one of ordinary skill would know that if the output would not be used, then their would be no reason for the signal to be sent to the status change factor supply;

since the signal is being send, it therefore must be used by [802] which would satisfy the limitation in the claim.

12. In response to the above-mentioned argument, applicant's interpretation of the prior art has been considered but they are not persuasive. The second reference, Rakib teaches a memory for storing tap factors corresponding to the plurality of statuses judged by said frequency information threshold device respectively. Rakib teaches the knowledge of having a memory to store tap factors based upon a plurality statuses that are judged via a threshold (See Paragraph [0592], "If it is not less than this threshold, the rotational amplifier has falsely locked, and processing proceeds to step 1538 to correct the situation by loading the SE main tap correction factor into the memory", where there are two different statuses based upon a threshold, and depending on that status storing tap factors). Although the applicant argues that the design of the memory would be different if it was to be used the same way as the application, this in fact is a design choice. Since the limitations in the claim are disclosed in the publication of Rakib, does not change how they are designed. The memory discloses storing the tap factors that are used to correct, which are the same as just tap factors. Any type of device that judges based upon thresholds can be considered the "frequency information threshold device". Therefore Rakib reference corrects the deficiencies that the AAPA fails to teach.

13. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention

where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

Drawings

14. Figure 8 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

15. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

16. Claim 1, 3 and 11 are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant Admitted Prior Art, for purposes of examination the publication US 2006/0072379 A1 will be used

17. Regarding claim 1, the applicant admitted prior art teaches an adaptive equalization circuit, comprising:

an analog-digital conversion device (See Figure 8, [101]) for sampling signals read from a recording medium (See Paragraph [0050], "which are signals read from the recording medium and sampled by the analog-digital conversion means");

a first digital equalization device (See Figure 8, [102]) for equalizing the-waveforms (See Paragraph [0052], "the data by the analog-digital conversion means 101 is equalized by the first digital equalization means 102") of first output signals from said analog-digital conversion device (See Figure 8, where the output of [101], the first output signal, is sent to [102]);

a phase synchronization device (See Figure 8, [103]) for synchronizing phases for second output signals from said first digital equalization device (See Figure 8, where [102], the second output signals, are sent to [103]);

an equalization target value generation device (See Figure 8, [1041]) for generating an equalization target value of said first digital equalization device from third output signals from said phase synchronization device (See Figure 8, where the output of [103], the third output signal, is sent to [1041]), and for outputting fourth output signals (See Figure 8, where [1041] outputs a signal, the fourth signal); and

a first factor computation device (See Figure 8, [802]) for receiving as input signals said first (See Figure 8, where the input of [802], the first factor computation device, has an input from [101] via a delay and [801]. Since the limitation does not state directly connected to the output of [101], the "first output" of [101] is used as an inputto

[802]), second (See Figure 8, where the input of [802], the first factor computation device, has an input from [102] via device [1031]. Since the limitation does not state directly connected to the output of [102], the "second output" of [102] is used as an input to [802]), and fourth output signals (See Figure 8, where the input of [802], the first factor computation device, has an input from [1041], the "fourth output" of [1041] is used as an input to [802]), and for computing tap factors of said first digital equalization device (See Paragraph, [0007], "the tap factors of the first digital equalization means 102 are computed by the temporary factor computation means 802") from said first, second, and fourth output signals (See Figure 8, as stated above, where the second is used to compute the tap factors, and all three signals are fed into the device [802], thus being "used" in some capacity).

18. Regarding claim 3, the applicant admitted prior art (See Paragraph [0045]) taught the adaptive equalization circuit according to claim 1, as described above. The applicant admitted art further teaches wherein said first digital equalization device is an FIR filter having tap factors of a symmetric type (See Paragraph [0086], "The first digital equalization means 102 is comprised of an FIR filter in the above description, but a new advantage is generated if this filter is constructed to be a tap factor symmetric type", Also See Figure 8, where [102] is considered prior art).

19. Regarding claim 11, the applicant admitted prior art teaches an adaptive equalization method for equalizing signals read from a recording medium to a desired characteristic, comprising:

reading first signals from a recording medium (See Paragraph [0050], "which are signal read from the recoding medium");

sampling said first signals (See Figure 8, [101], also see Paragraph [0050], "which are signals read from the recording medium and sampled by the analog-digital conversion means") and outputting sampled second signals (See Figure 8, [101] the output);

equalizing waveforms for the sampled second .signals (See Figure 8, [102]) and outputting waveform-equalized third signals (See Figure 8, the output of [102]);

performing phase synchronization for the waveform-equalized third signals (See Figure 8, [103], where the equalized waveform signals are being input) and outputting phase-synchronized fourth signals (See Figure 8, the output of [103]);

generating a fifth signal (See Figure 8, the output from [1041]) from the phase-synchronized fourth signals (See Figure 8, where the output of [103] being the fourth signal which are input to [1041]), said fifth signal corresponding to an equalization target value of said waveform equalization (See Paragraph [0067], "the temporary target value, which is the equalization target value");;

receiving said second (See Figure 8, where the input to [802] receives the "second signal" from the output of [101], via outputs of the "delay" and [801]. Since the limitation does not state directly connected to the output of [101], the "second output

signal" of [101] is used as an input to [802]), fourth (See Figure 8, where the input to [802] receives the "fourth signal" from the output of [103]), and fifth signals (See Figure 8, where the input to [802] receives the "fifth signal" from the output of [1041]) as inputs to a first factor computation device (See Figure 8, [802]); and

computing tap factors (See Paragraph, [0007], "the tap factors of the first digital equalization means 102 are computed by the temporary factor computation means 802") with said first factor computation device (See Figure 8, [802]) for said waveform equalization from said second, fourth, and fifth signals (See Figure 8, as stated above, where the fourth signal is used to compute the tap factors, and all three signals are fed into the device [802], thus being "used" in some capacity).

Claim Rejections - 35 USC § 103

20. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 2, 6 and 12 are rejected under 35 U.S.C. 103(a) as being obvious over applicant admitted art (Figure 8), in view of US 2002/0067677 A1 by Miyashita et al.

21. Regarding claim 2, applicant admitted prior art (See Paragraph [0045]) taught the adaptive equalization circuit according to claim 1, as described above. The applicant admitted art further teaches wherein said equalization target value generation device further comprises:

a temporary target value generation device for generating a temporary target value (See Figure 8, [1041]. Also See Paragraph [0097], "temporary target values

determined by the temporary target value generation means 1041"), that is the equalization target value of the phase-synchronized signals (See Paragraph [0067] "For example, in the temporary target value generation means 1041, the temporary target value, which is the equalization target value with the re-sampling frequency");

but does not teach an equalization target phase rotation device for generating a true target value, from said temporary target value, the true target value being an equalization target value before synchronizing phases by said phase synchronization device.

22. Miyashita teaches the knowledge of an equalization target phase rotation device (See Figure 10, [113]) for generating a true target value (See Paragraph [0129]) from a temporary target values (See Figure 10, "Temporary Judgment Output" as the input to [113]), before, or never, phase synchronization occurs (See Figure 10, where the signal never has phase synchronization performed to it. Also see Paragraph [0112]), is well known in the art.

23. It would have been obvious to one of ordinary skill in the art, having the teachings of the applicant admitted prior art and Miyashita before them at the time the invention was made, to modify the teachings of the applicant admitted prior art to further include teach an equalization target phase rotation device for generating a true target value, that is an equalization target value before synchronizing phases by said phase synchronization device, from said temporary target value. In order to determine the true target value, the process can require indirectly using phase synchronization by using the temporary target value that was determined from the signal after phase

synchronization, thus makes the desired result closer to the "true" target value. One of ordinary skill in the art would therefore have been motivated to make the modification of an equalization target phase rotation device for generating a true target value from a temporary target values, before, or never, phase synchronization occurs.

24. Regarding claim 6, the applicant admitted prior art (See Paragraph [0045]) together with Miyashita taught the adaptive equitation circuit according to claim 2, as described above. The applicant admitted further teaches wherein said phase synchronization device is a phase synchronization loop comprising a first interpolation device for interpolating the second output signals from said first digital equalization device (See Figure 8, [103]. Also See Paragraph [0022], "the phase synchronization means is a phase synchronization loop further comprising first interpolation means for interpolating signals equalized by the first digital equalization means") and an interpolation position computation device for computing an interpolation position of said first interpolation device from sixth output signals from said first interpolation device (See Figure 8, [1032]. Also See Paragraph [0022], "interpolation position computation means for computing an interpolation position of the first interpolation means from the output of the first interpolation means"), the interpolation position of said second interpolation device being computed by said interpolation position computation device (See Figure 8, [1032]. Also See Paragraph [0022], "and the interpolation position of the second interpolation means is computed by the interpolation position computation means". Although it is not taught in figure 8, to have a second interpolation means, it is

disclosed that the interpolation position computation means performs a task that is not used), is it not taught said equalization target phase rotation device being a second interpolation device for interpolating said temporary target value and acquiring said true target value.

25. Miyashita taught the said equalization target phase rotation device as described in claim 2 above. Miyashita further teaches where the "said equalization target phase rotation device" (See Figure 10, [113]) is a second interpolation device (See Paragraph [0112], "In the table, the corresponding relationships between the input values and the output values are defined on the basis of the state transition diagram (FIG. 11)") for interpolating said temporary target value (See Figure 10, input to [113] "Temporary judgment output") and acquiring said true target value.(See Paragraph [0113] through [0122]).

26. Regarding claim 12, the applicant admitted prior art teaches an adaptive equalization method for equalizing signals read from a recording medium to a desired characteristic, comprising:

reading first signals from a recording medium (See Paragraph [0050], "which are signal read from the recoding medium");

sampling the read first signals (See Figure 8, [101], also see Paragraph [0050], "which are signals read from the recording medium and sampled by the analog-digital conversion means") and generating sampled second signals (See Figure 8, [101] the output);

equalizing waveforms (See Figure 8, [102], Also see Paragraph [0052], "the data by the analog-digital conversion means 101 is equalized by the first digital equalization means 102") for the sampled second signals (See Figure 8, where the output of [101] is the "sampled second signals", which are fed into [102]) and generating waveform-equalized third signals (See Figure 8, the output of [102] being the "third signals");

performing phase synchronization (See Figure 8, [103]) for the waveform-equalized third signals (See Figure 8, where the output of [102] is the "waveform-equalized third signals", which are fed into [103]) and generating phase-synchronized fourth signals (See Figure 8, the output of [103] being the "fourth signals");

generating a temporary target value (See Figure 8, [1041]) that is an equalization target value (See Paragraph [0067], "the temporary target value, which is the equalization target value") of the phase-synchronized fourth signals (See Figure 8, where the output of [103] is the "phase-synchronized fourth signals" which are fed into [1041]) and generating a fifth signal corresponding to the temporary target value (See Figure 8, the output of [1041] being the "fifth signal"); and

computing tap factors (See Figure 8, [802]) for said waveform equalization from said sampled second signals (See Figure 8, where the input to [802] receives the "second signal" from the output of [101], via outputs of the "delay" and [801]. Since the limitation does not state directly connected to the output of [101], the "second signal" of [101] is used as an input to [802]), and said waveform-equalized third signals (See Figure 8, where the input to [802] receives the "third signal" from the output of [102], via output of [1031]. Since the limitation does not state directly connected to the output of

[102], the "third signal" of [102] is used as an input to [802]), and teaches using target values to generate the tap factor (See Figure 8, the output of [1041]), but does not teach

generating a true target value from said fifth signal, the true target value being an equalization target value before performing phase synchronization, and generating a sixth signal corresponding to the true target value.

Miyashita teaches the knowledge of generating an equalization target value (See Figure 10, [113]) from a temporary target values (See Figure 10, "Temporary Judgment Output" as the input to [113]), before, or never, phase synchronization occurs (See Figure 10, where the signal never has phase synchronization performed to it. Also see Paragraph [0112]), is well known in the art.

27. It would have been obvious to one of ordinary skill in the art, having the teachings of the applicant admitted prior art and Miyashita before them at the time the invention was made, to modify the teachings of the applicant admitted prior art to further include to generate a true target value, that is an equalization target value before performing phase synchronization, from said temporary target value. In order to determine the true target value, the process can require indirectly using phase synchronization by using the temporary target value that was determined from the signal after phase synchronization, thus makes the desired result closer to the "true" target value. One of ordinary skill in the art would therefore have been motivated to make the modification so to generate an equalization target value from a temporary target values, before, or never, phase synchronization occurs.

28. Claim 14 is rejected under 35 U.S.C. 103(a) as being obvious over applicant admitted art (Figure 8) in view of US 2003/0156603 A1 by Rakib et al.

29. Regarding claim 14, the applicant admitted prior art (See Paragraph [0045]) teaches an adaptive equalization circuit, comprising:

an analog-digital conversion device (See Figure 8, [101]) for sampling signals read from a recording medium (See Paragraph [0050], "which are signals read from the recording medium and sampled by the analog-digital conversion means");

a first digital equalization device (See Figure 8, [102]) for equalizing waveforms of output of said analog-digital conversion device (See Paragraph [0052], "the data by the analog-digital conversion means 101 is equalized by the first digital equalization means 102");

a phase synchronization device (See Figure 8, [103]) for synchronizing phases for signals equalized by said first digital equalization device;

a frequency information threshold device (See Figure 4, [402], where Figure 4 is depicting [1032] of Figure 8, which is prior art) for judging frequency information of said phase synchronization device in a plurality of statuses using one or more threshold values (See Paragraph [0073]);

a status change factor supply device (See Figure 8, [802]) for supplying a tap factor (See Paragraph [0007], "the tap factors of the first digital equalization means 102 are computed by the temporary factor computation means 802 ") corresponding to said status to said first digital equalization device when the status judged by said frequency

information threshold device changes (See Figure 8, where the inputs to [802] are from the first digital equalization device [102] and from frequency information threshold device [1032], that contains [402]), but does not teach

a second memory for previously storing tap factors corresponding to the plurality of statuses judged by said frequency information threshold device respectively. Rakib teaches the knowledge of having a memory to store tap factors based upon a plurality statuses that are judged via a threshold (See Paragraph [0592], "If it is not less than this threshold, the rotational amplifier has falsely locked, and processing proceeds to step 1538 to correct the situation by loading the SE main tap correction factor into the memory", where there are two different statuses based upon a threshold, and depending on that status storing tap factors), is well known in the art.

30. It would have been obvious to one of ordinary skill in the art, having the teachings of the applicant admitted prior art and Rakib before them at the time the invention was made, to modify the teachings of the applicant admitted prior art to further include a second memory for previously storing tap factors corresponding to the plurality of statuses judged by said frequency information threshold device respectively. Once the tap factors have been determined from the frequency information threshold device, the tap factors would be stored, thus making it useful by other devices within the circuit to use at a later time. One of ordinary skill in the art would therefore have been motivated to make the modification so to include a memory to store tap factors based upon a plurality statuses that are judged via a threshold.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian J. Stevens whose telephone number is (571)270-3623. The examiner can normally be reached on M-F 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BS
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